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PTO/SB/21 (04-07)
Approved for use through 09/30/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

	Application Number	10/821,466				
TRANSMITTAL	Filing Date	April 8, 2004				
FORM	First Named Inventor	Yu, et al.				
	Art Unit	2825				
(to be used for all correspondence after initial f	Examiner Name	Mr. Paul Dinh				
Total Number of Pages in This Submission	Attorney Docket Number	A1168				
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	ENCLOSURES (Check al	I that apply)				
Fee Transmittal Form	Drawing(s)	After Allowance Communication to TC				
Fee Attached	Licensing-related Papers	Appeal Communication to Board of Appeals and Interferences				
Amendment/Repty	Petition Retition to Convert to a	Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)				
After Final	Petition to Convert to a Provisional Application	Proprietary Information				
Affidavits/declaration(s)	Power of Attorney, Revocation Change of Correspondence					
Extension of Time Request	Terminal Disclaimer	Other Enclosure(s) (please Identify below):				
Express Abandonment Request	Request for Refund	Certificate of Correction Return Receipt Postcard				
Information Disclosure Statement	CD, Number of CD(s)	·				
	Landscape Table on C	D				
Certified Copy of Priority Document(s)	Remarks					
Reply to Missing Parts/	Zunhang Yu, not Zunghang Yu as currently shown. ion on the issued patent.					
Incomplete Application						
under 37 CFR 1.52 or 1.53		Certificate				
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	URE OF APPLICANT, ATTO	RNEY, OR AGENT "71 1 1 2007				
Firm Name Altera Corporation	//	Certificate MAY 1 1 2007 Of Correction				
Signature Flaind						
Printed name Elaine K. Lee						
Date May (, 2.007 Reg. No. 41,936						
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I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:						
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PTO/SB/17 (02-07)
Approved for use through 02/28/2007. OMB 0651-0032
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Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL			Applicat	on Number	10/821,466				
			Filing Da		April 8, 2004				
	For FY	2007		First Na	med Inventor	Yu, et al.	•		
Applicant claims small entity status. See 37 CFR 1.27			Examine	r Name	Mr. Paul Dinh				
		1		Art Unit		2825			
TOTAL AMOUNT	OF PAYMENT	(\$)	100.00	Attorney	Attorney Docket No. A1168				
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FEE CALCULA	TION								
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3. APPLICATION SIZE FEE									
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50									
sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
Total Sheets Extra Sheets Number of each additional 50 or fraction thereof Fee (\$) Fee Paid (\$)									
100 = / 50 = (round up to a whole number) x =									
4. OTHER FEE(S) Non-English Specification, \$130 fee (no small entity discount) Fees Paid (\$)									
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Signature	411/1			Registration	on No. ent) 41,936		Telephone /	108-544-7591	
<u> </u>	Clare	in	<u> </u>	(Attorney/A	jent) 41,550			au (, 2007	
Name (Print/Type) E	laine K. Lee						Date M	Uu 1 ////CFT	

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(12) United States Patent Yu et al.

(10) Patent No.:

US 7,178,117 B1

(45) Date of Patent:

Feb. 13, 2007

(54) APPARATUS AND METHOD FOR RTL BASED FULL CHIP MODELING OF A PROGRAMMABLE LOGIC DEVICE

(75) Inventors: Zunghang Yu, Sunnyvale, CA (US); Ninh Ngo, San Jose, CA (US); Guy Dupenloup, Redwood City, CA (US)

(73) Assignee: Altera Corporation, San Jose, CA

(US)

Subject to any disclaimer, the term of this patent is extended or adjusted under 35

U.S.C. 154(b) by 170 days.

(21) Appl. No.: 10/821,466

Notice:

(22) Filed: Apr. 8, 2004

(51) Int. Cl. G06F 17/50 (2006.01) G06F 9/45 (2006.01) H03K 17/693 (2006.01)

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U.S. PATENT DOCUMENTS

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Primary Examiner—Paul Dinh Assistant Examiner—Suresh Memula

(57) ABSTRACT

An RTL representation for a LAB is generated. A full chip RTL model is then generated using a plurality of the LAB RTLs. Using the full chip RTL model, a full chip simulation of the PLD chip is performed to verify and debug the electronic design.

15 Claims, 10 Drawing Sheets

Zunhang Yu

